ABSTRACT

A method of fabricating a CMOS inverter including providing a heterostructure having a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on the Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer; and integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of the nMOSFET are formed in the strained surface layer. Another embodiment provides a method of fabricating an integrated circuit including providing a heterostructure having a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on the Si substrate, and a strained layer on the relaxed $Si_{1-x}Ge_x$ layer; and forming a p transistor and an n transistor in the heterostructure, wherein the strained layer comprises the channel of the n transistor and the p transistor, and the n transistor and the p transistor are interconnected in a CMOS circuit.